FIG.1

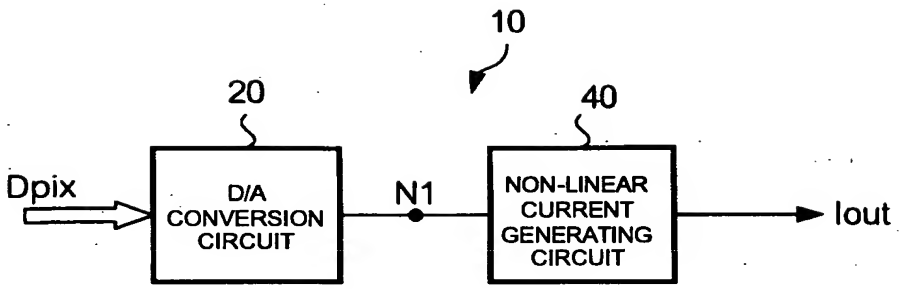
10
20
40
Dpix
D/A CONVERSION CIRCUIT
N1
NON-LINEAR CURRENT GENERATING CIRCUIT
Iout

FIG.2

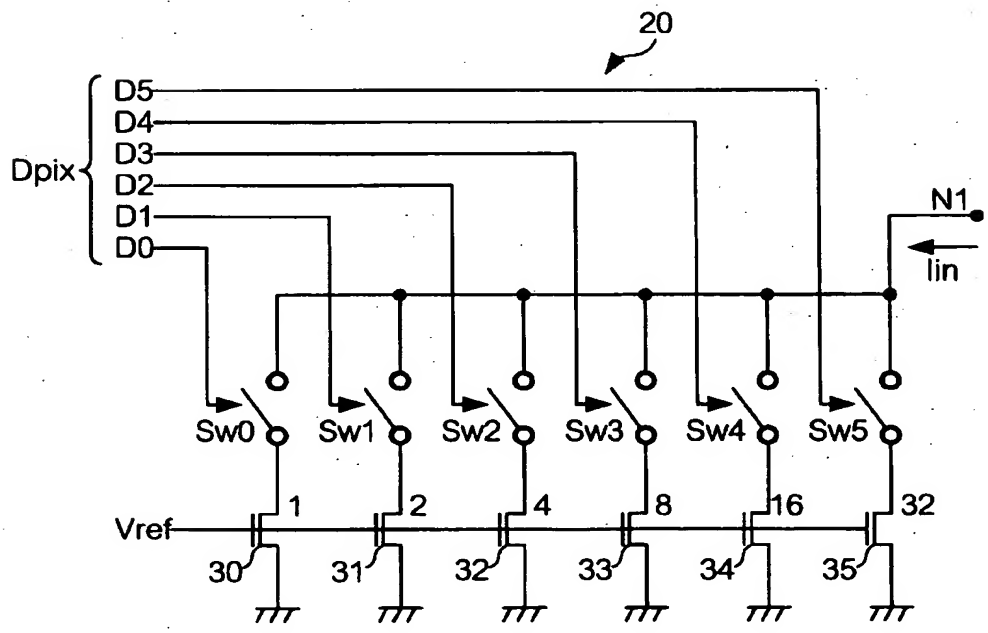
20
D5
D4
D3
D2
D1
D0
Dpix
N1
Iin
Sw0
Sw1
Sw2
Sw3
Sw4
Sw5
Vref
1
2
4
8
16
32
30
31
32
33
34
35

FIG.3

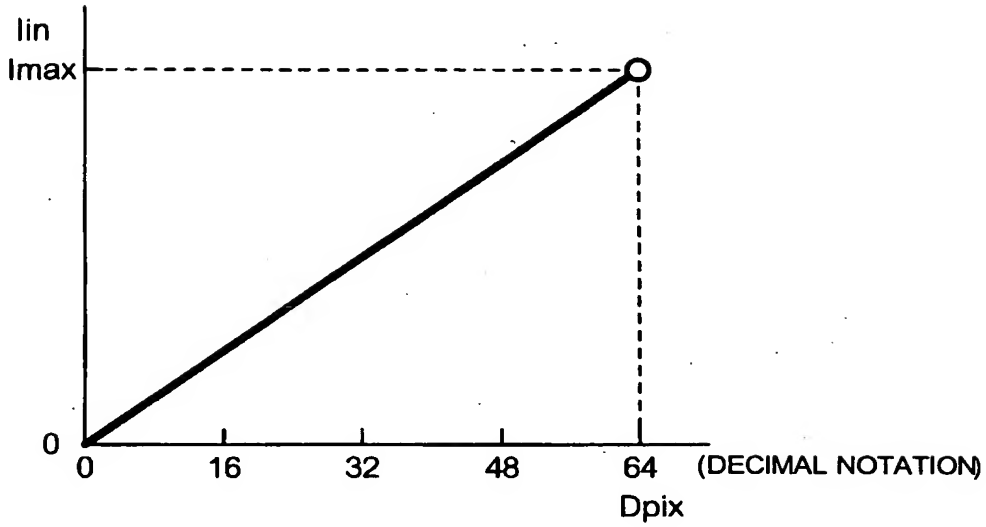
Iin
Imax
0
0
16
32
48
64
Dpix
(DECIMAL NOTATION)

FIG.4

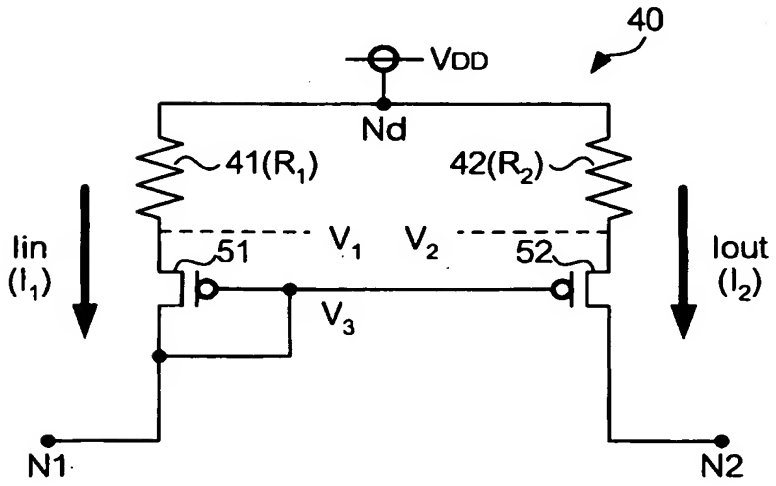
40
VDD
Nd
41(R1)
42(R2)
Iin
(I1)
51
V1
V2
52
Iout
(I2)
V3
N1
N2

FIG.5

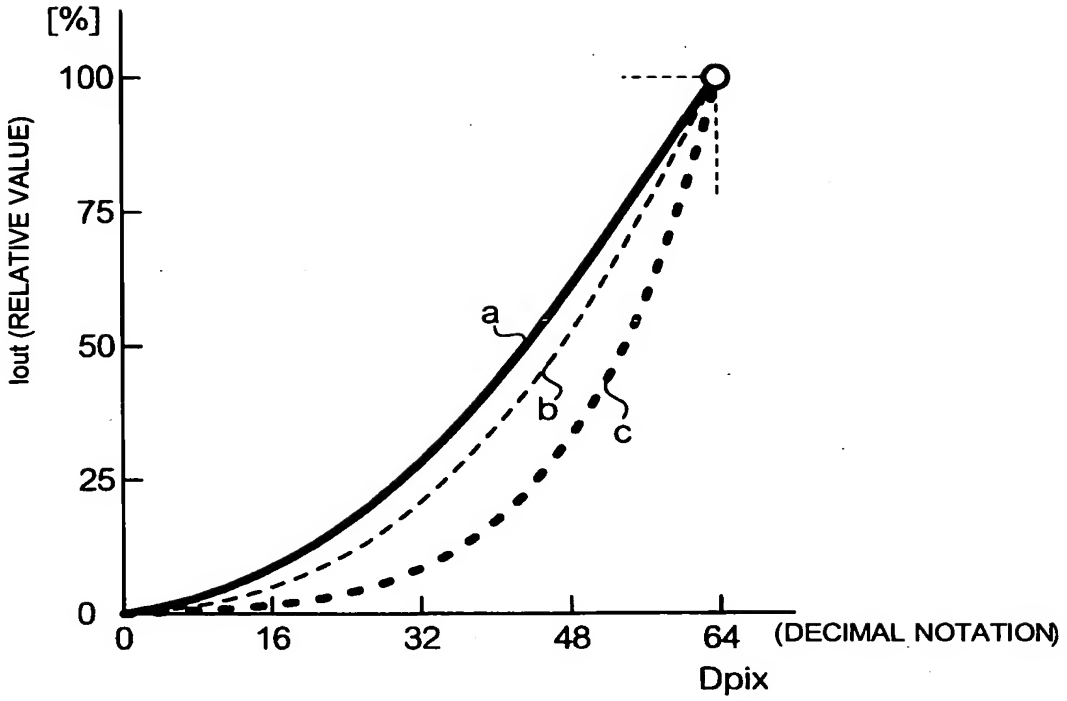

FIG.6

$$\sqrt{\frac{2I_1}{\beta_1}} = V_2 - I_1 \bullet R_1 + I_2 \bullet R_2 - V_3 - V_{th}$$

$$\therefore I_1 \bullet R_1 - I_2 \bullet R_2 + \sqrt{\frac{2I_1}{\beta_1}} = V_2 - V_3 - V_{th} \cdots\cdots (7)$$

FIG.7

$$I_2 = \frac{1}{2}\beta_2\left(I_1 \bullet R_1 - I_2 \bullet R_2 + \sqrt{\frac{2I_1}{\beta_1}}\right)^2$$

$$\therefore \frac{2I_2}{\beta_2} = (I_1 \bullet R_1 - I_2 \bullet R_2)^2 + 2(I_1 \bullet R_1 - I_2 \bullet R_2)\sqrt{\frac{2I_1}{\beta_1}} + \frac{2I_1}{\beta_1}$$

$$= I_1^2 \bullet R_1^2 - 2I_1 \bullet R_1 \bullet I_2 \bullet R_2 + I_2^2 \bullet R_2^2 + 2I_1 \bullet R_1\sqrt{\frac{2I_1}{\beta_1}} - 2I_2 \bullet R_2\sqrt{\frac{2I_1}{\beta_1}} + \frac{2I_1}{\beta_1}$$

$$\therefore \quad R_2^2 \bullet I_2^2 - 2\left(\frac{1}{\beta_2} + I_1 \bullet R_1 \bullet R_2 + R_2\sqrt{\frac{2I_1}{\beta_1}}\right)I_2 + \left(\sqrt{\frac{2I_1}{\beta_1}} + I_1 \bullet R_1\right)^2 = 0 \cdots\cdots (8)$$

FIG.8

$$I_2=\frac{\dfrac{1}{\beta_2}+I_1\bullet R_1\bullet R_2+R_2\sqrt{\dfrac{2I_1}{\beta_1}}+\sqrt{\left(\dfrac{1}{\beta_2}+I_1\bullet R_1\bullet R_2+R_2\sqrt{\dfrac{2I_1}{\beta_1}}\right)^2-R_2^2\left(\sqrt{\dfrac{2I_1}{\beta_1}}+I_1\bullet R_1\right)^2}}{R_2^2}\cdots(9)$$

FIG.9

$$I_2 = \frac{1}{2}\beta_2\left(\sqrt{\frac{2I_1}{\beta_1}} + I_1 \bullet R_1\right)^2 \cdots\cdots (10)$$

FIG.10

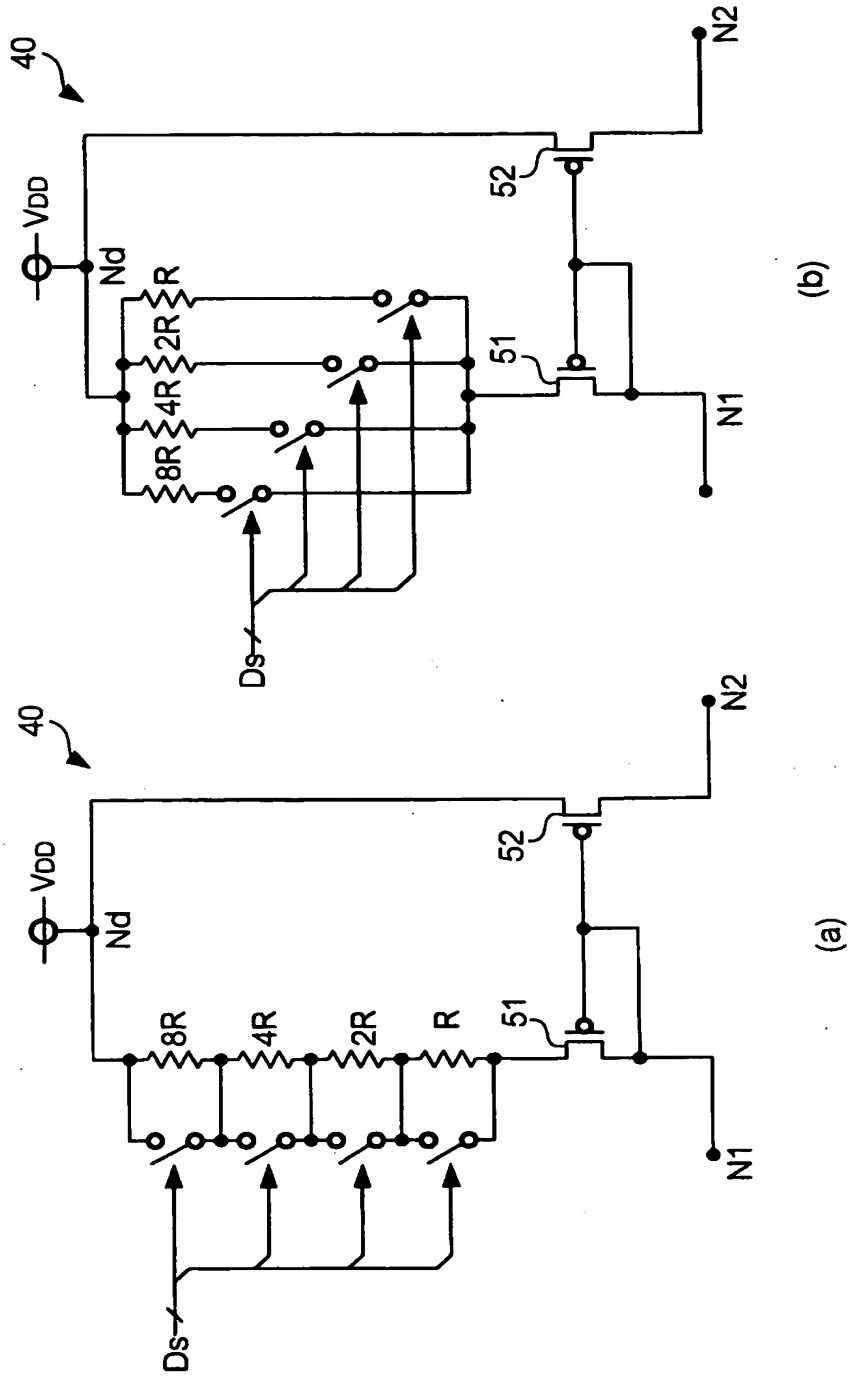
40
N2
52
VDD
Nd
R
2R
4R
8R
51
N1
Ds
(b)
40
N2
52
VDD
Nd
8R
4R
2R
R
51
N1
Ds
(a)

FIG.11

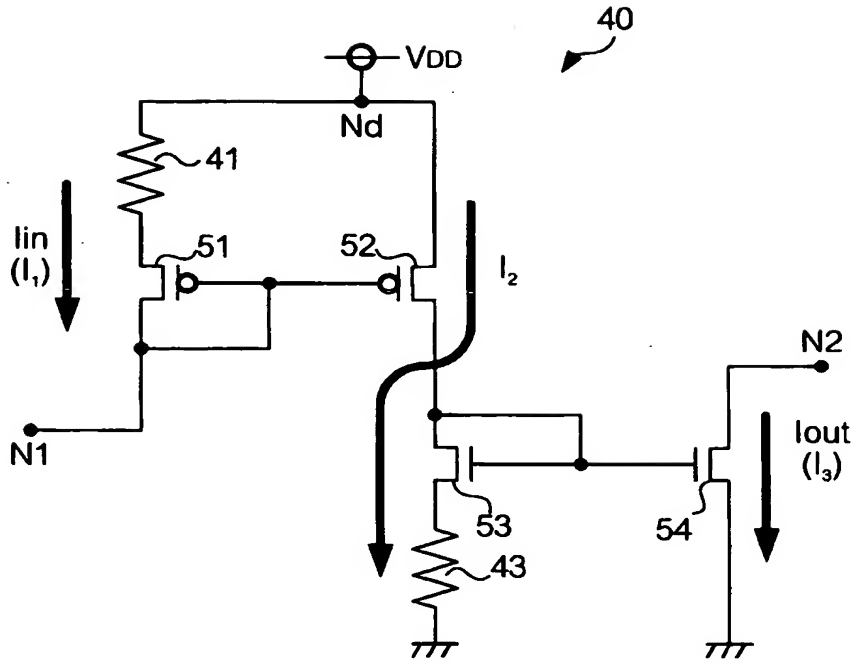

FIG.12

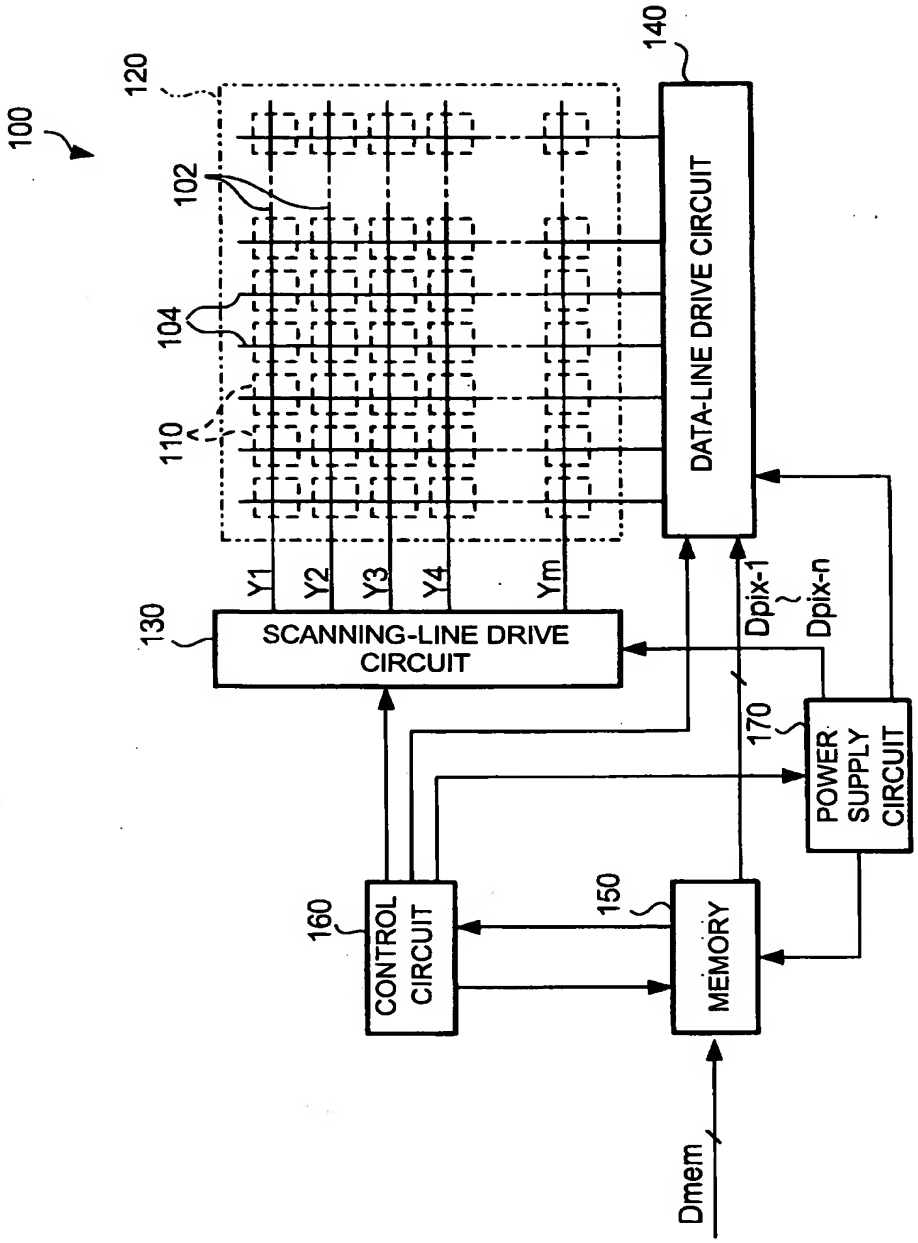
100
120
102
104
110
140
DATA-LINE DRIVE CIRCUIT
Y1
Y2
Y3
Y4
Ym
130
SCANNING-LINE DRIVE CIRCUIT
Dpix-1
Dpix-n
170
POWER SUPPLY CIRCUIT
160
CONTROL CIRCUIT
150
MEMORY
Dmem

FIG.13

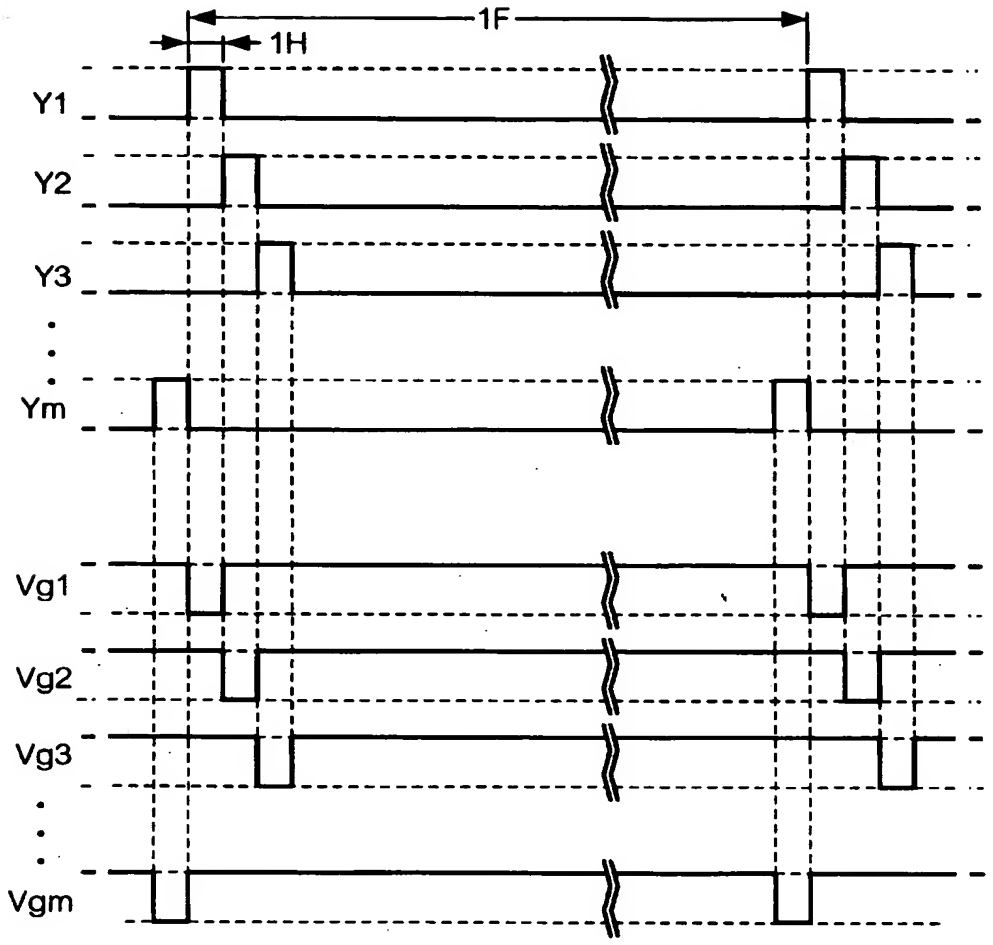

FIG.14

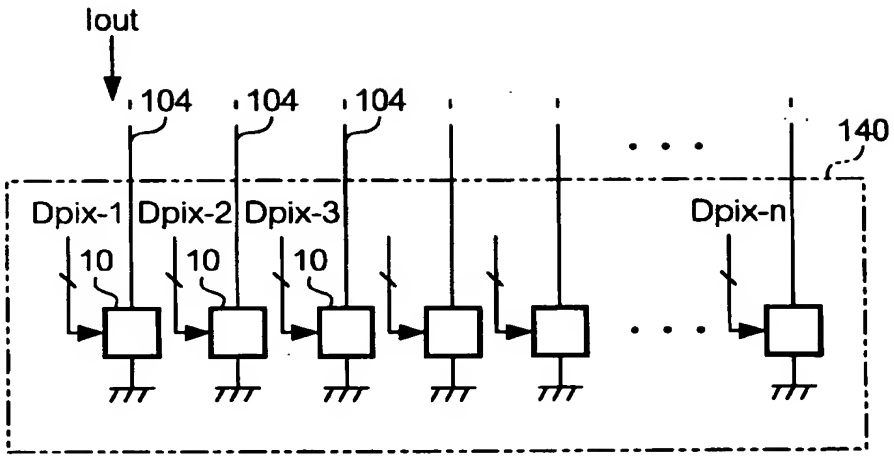

FIG.15

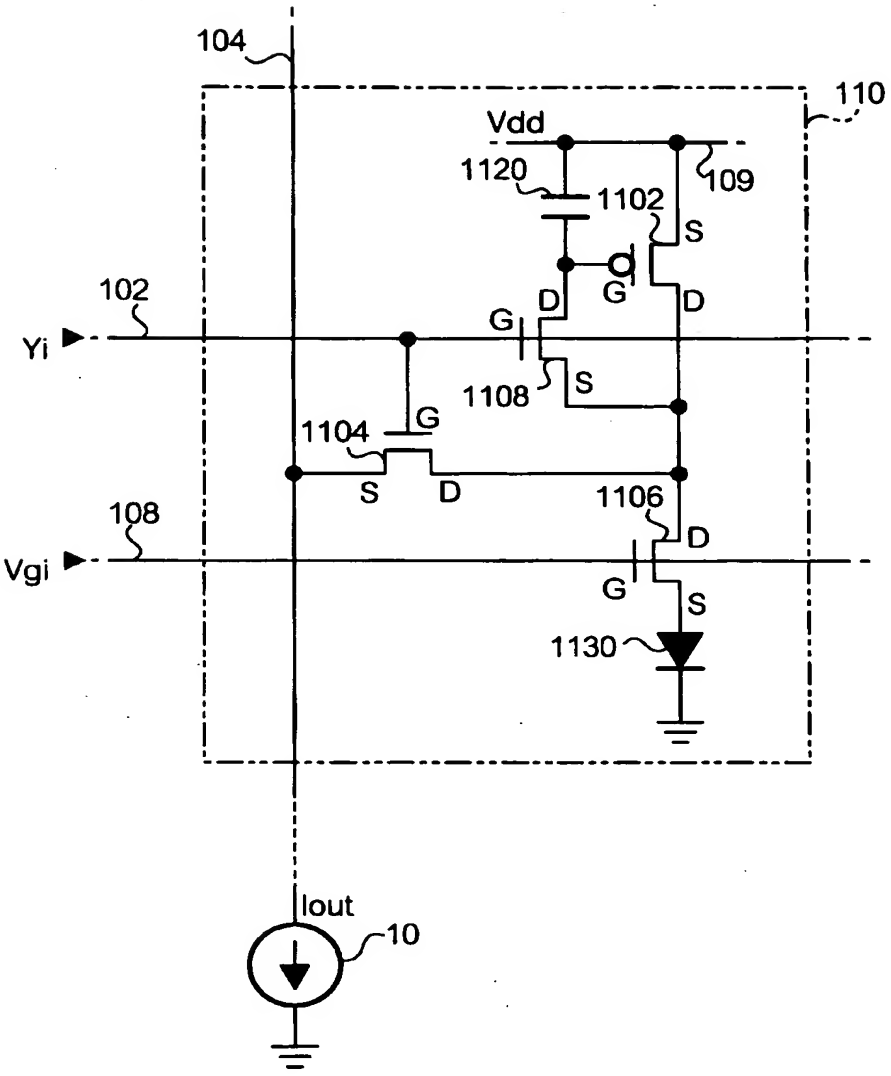
104
110
Vdd
1120
1102
109
S
G
D
D
G
102
Yi
G
1108
S
1104
G
S
D
1106
D
108
Vgi
G
S
1130
Iout
10

FIG.16

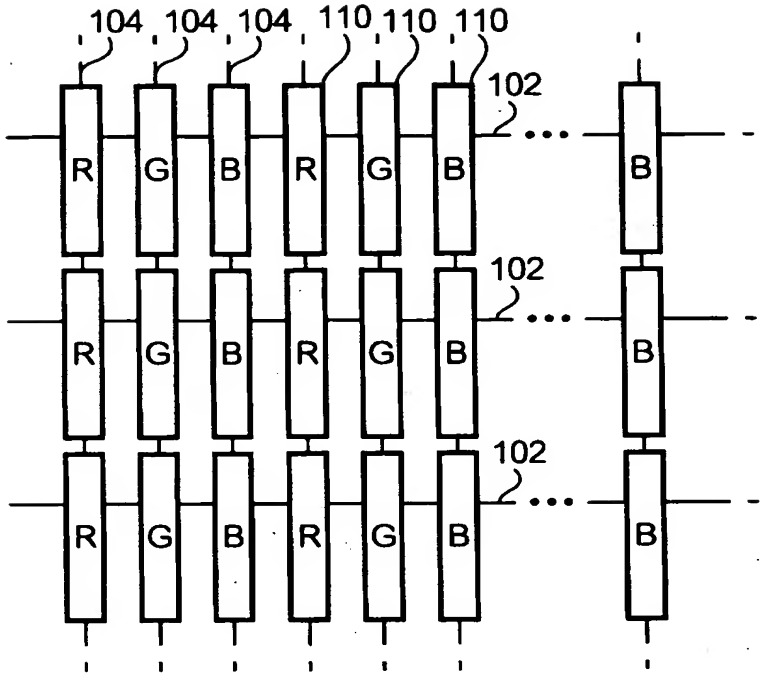

FIG.17

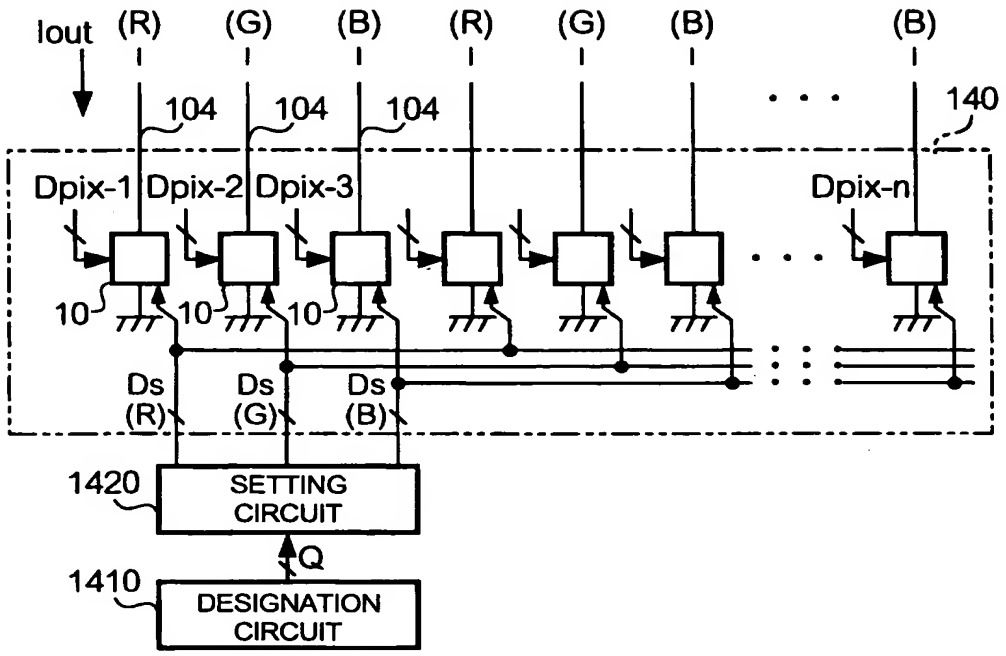
Iout
(R)
(G)
(B)
(R)
(G)
(B)
(B)
104
104
104
140
Dpix-1
Dpix-2
Dpix-3
Dpix-n
10
10
10
Ds (R)
Ds (G)
Ds (B)
1420
SETTING CIRCUIT
Q
1410
DESIGNATION CIRCUIT

FIG.18

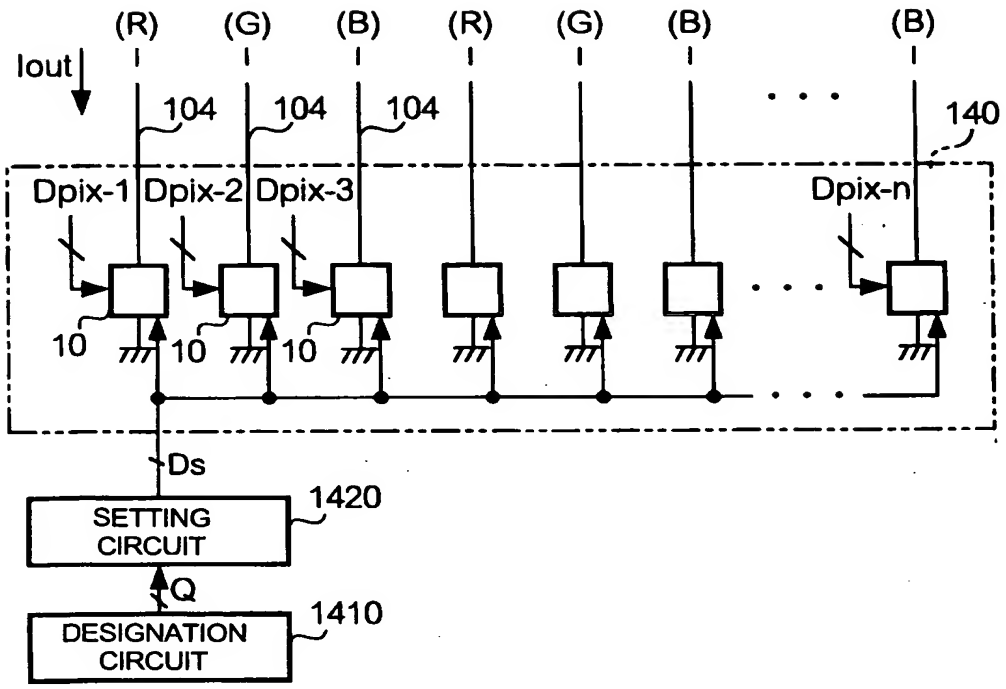
(R)
(G)
(B)
(R)
(G)
(B)
(B)
Iout
104
104
104
140
Dpix-1
Dpix-2
Dpix-3
Dpix-n
10
10
10
Ds
SETTING CIRCUIT
1420
Q
DESIGNATION CIRCUIT
1410

FIG.19

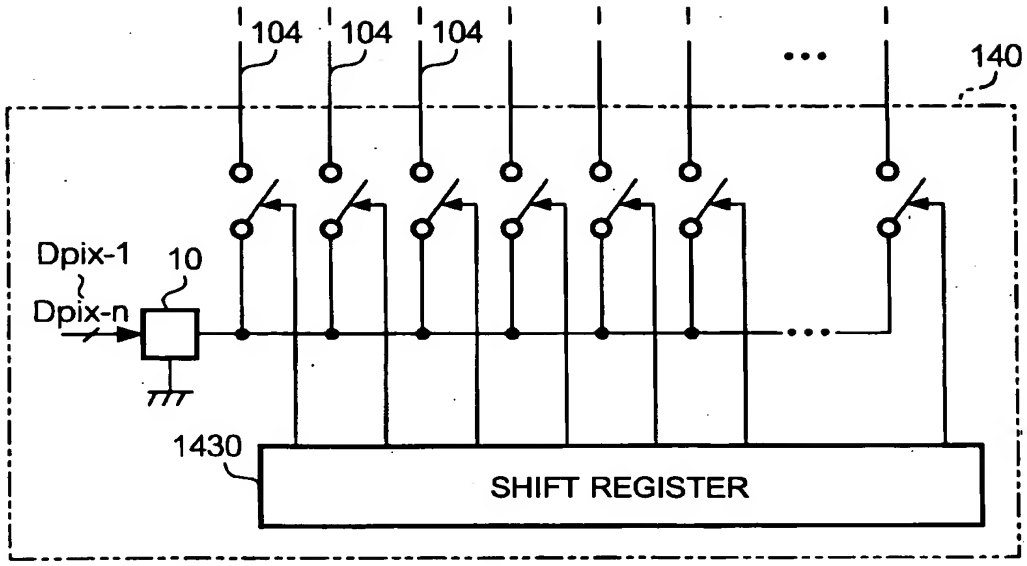
104
104
104
140
Dpix-1
Dpix-n
10
1430
SHIFT REGISTER

FIG.20

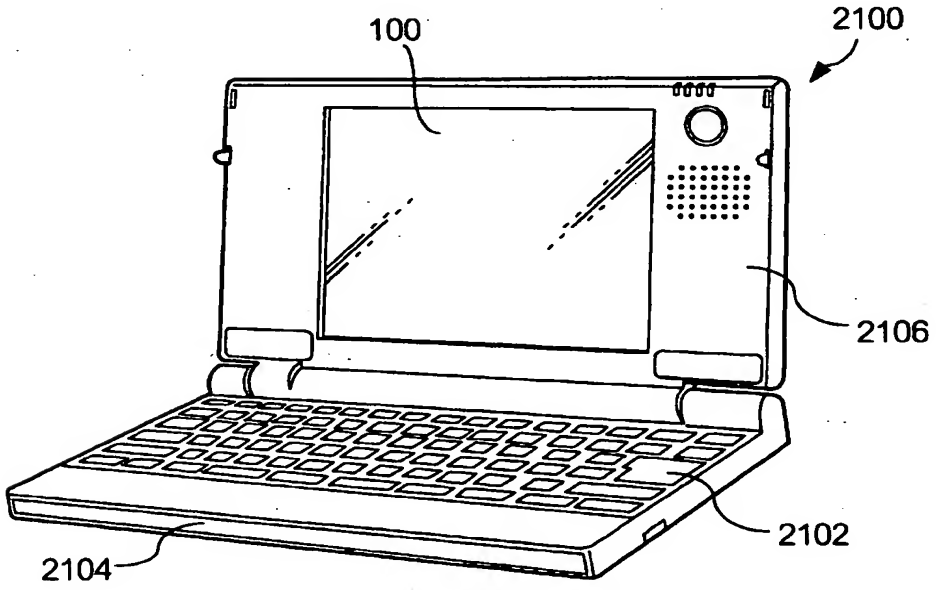
100
2100
2106
2102
2104

FIG.21

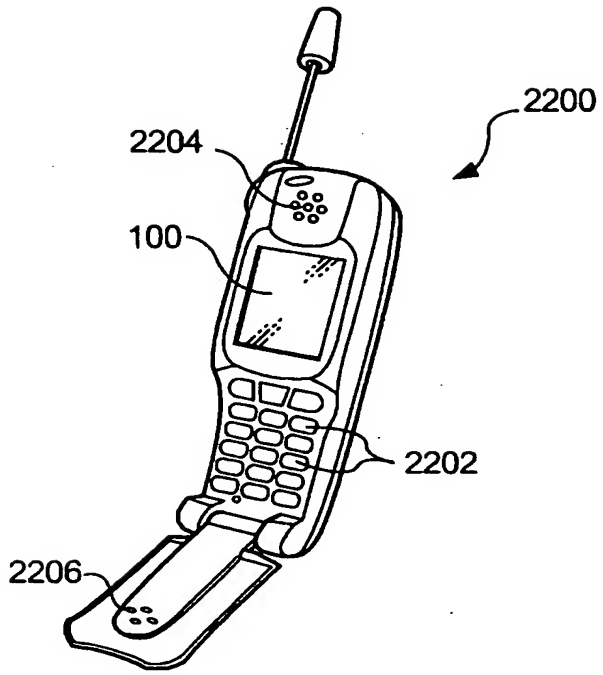

FIG.22